Amendments to the Claims

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently amended) A method of reducing power consumption in an *N*-way ~~a multi-way~~ set-associative cache memory having *Y* sets, wherein *N* is a first integer, and wherein *Y* is a second integer, the method comprising:

during a first clock cycle *k*, in response to an address, identifying an associated set in the cache memory, comparing the address to respective tag portions of *N* blocks in the associated set, and outputting a signal in response thereto, wherein *k* is an integer; and

during a second clock cycle *k*+1, in response to the signal indicating that ~~a match between~~ one of the *N* blocks in the associated set is a match with ~~and~~ the address, reading a non-tag portion of the matching block in the associated set, while non-tag portions of *N*-1 non-matching blocks ~~a non-matching block~~ in the associated set are ~~is~~ disabled, and while non-tag portions of *Y*-1 non-associated sets are disabled.

2. (Previously presented) The method of Claim 1, wherein the reading comprises:

enabling the non-tag portion of the matching block in the associated set.

3. (Previously presented) The method of Claim 2, wherein the enabling comprises:

applying power to the non-tag portion of the matching block in the associated set.

4. (Currently amended) The method of Claim 1, and comprising:

removing power from at least one of the non-tag portions of: the *N*-1 non-matching blocks ~~block~~ in the associated set; and the *Y*-1 non-associated sets.

5. (Currently amended) The method of Claim 4, wherein the removing ~~power~~ comprises:

removing power from the at least one of the non-tag portions ~~the non-matching block in the associated set~~, so that it ~~the non-matching block in the associated set~~ is disabled from outputting information, and so that it ~~the non-matching block in the associated set~~ continues to store the information.

6. (Previously presented) The method of Claim 1, wherein the cache memory is a program cache.

7. (Previously presented) The method of Claim 1, wherein the cache memory is a data cache.

8. (Currently amended) The method of Claim 1, wherein the comparing ~~the address~~ comprises:

comparing a portion of the address to respective tag portions of the *N* blocks in the associated set.

9. (Currently amended) The method of Claim 1, wherein the reading ~~the non-tag portion~~ comprises:

reading the non-tag portion of the matching block in the associated set, while the non-tag portions of the *N*-1 non-matching blocks ~~block~~ in the associated set are ~~is~~ at least partly disabled, and while the non-tag portions of the *Y*-1 non-associated sets are at least partly disabled.

10. (Currently amended) The method of Claim 1, and comprising ~~wherein reading the non-tag portion comprises~~:

during the second clock cycle k+1, in response to a second address, identifying a second associated set in the cache memory, comparing the second address to respective tag portions of N blocks in the second associated set, and outputting a second signal in response thereto; and

during a third clock cycle k+2, in response to the second signal indicating that one of the N blocks in the second associated set is a match with the second address, reading a non-tag portion of the matching block in the second associated set, while non-tag portions of N-1 non-matching blocks in the second associated set are disabled, and while non-tag portions of Y-1 non-associated sets are disabled ~~reading the non-tag portion of the matching block in the associated set, while at least first and second non-matching blocks in the associated set are disabled~~.

11. (Currently amended) A system for reducing power consumption in an N-way ~~a multi-way~~ set-associative cache memory having Y sets, wherein N is a first integer, and wherein Y is a second integer, the system comprising:

first circuitry for: during a first clock cycle k, in response to an address, identifying an associated set in the cache memory, comparing the address to respective tag portions of N blocks in the associated set, and outputting a signal in response thereto, wherein k is an integer; and

second circuitry for: during a second clock cycle k+1, in response to the signal indicating that ~~a match between~~ one of the N blocks in the associated set is a match with ~~and~~ the address, reading a non-tag portion of the matching block in the associated set, while non-tag portions of N-1 non-matching blocks ~~a non-matching block~~ in the associated set are ~~is~~ disabled, and while non-tag portions of Y-1 non-associated sets are disabled.

12. (Previously presented) The system of Claim 11, wherein the second circuitry is for enabling the non-tag portion of the matching block in the associated set.

13. (Previously presented) The system of Claim 12, wherein the second circuitry is for applying power to the non-tag portion of the matching block in the associated set.

14. (Currently amended) The system of Claim 11, wherein the second circuitry is for removing power from at least one of the non-tag portions of: the *N*-1 non-matching blocks ~~block~~ in the associated set; and the *Y*-1 non-associated sets.

15. (Currently amended) The system of Claim 14, wherein the second circuitry is for removing power from the at least one of the non-tag portions ~~the non-matching block in the associated set~~, so that it ~~the non-matching block in the associated set~~ is disabled from outputting information, and so that it ~~the non-matching block in the associated set~~ continues to store the information.

16. (Previously presented) The system of Claim 11, wherein the cache memory is a program cache.

17. (Previously presented) The system of Claim 11, wherein the cache memory is a data cache.

18. (Currently amended) The system of Claim 11, wherein the first circuitry is for comparing a portion of the address to respective tag portions of the *N* blocks in the associated set.

19. (Currently amended) The system of Claim 11, wherein the second circuitry is for reading the non-tag portion of the matching block in the associated set, while the non-tag portions of the *N*-1 non-matching blocks ~~block~~ in the associated set are ~~is~~ at least partly disabled, and while the non-tag portions of the *Y*-1 non-associated sets are at least partly disabled.

20. (Currently amended) The system of Claim 11, wherein:

the first circuitry is for, during the second clock cycle k+1, in response to a second address, identifying a second associated set in the cache memory, comparing the second address to respective tag portions of N blocks in the second associated set, and outputting a second signal in response thereto; and

the second circuitry is for, during a third clock cycle k+2, in response to the second signal indicating that one of the N blocks in the second associated set is a match with the second address, reading a non-tag portion of the matching block in the second associated set, while non-tag portions of N-1 non-matching blocks in the second associated set are disabled, and while non-tag portions of Y-1 non-associated sets are disabled ~~reading the non-tag portion of the matching block in the associated set, while at least first and second non-matching blocks in the associated set are disabled~~.